(SP2T) LOW INSERTION LOSS SWITCH, DC-20 GHz

Model: LF-SP2T-20-GA

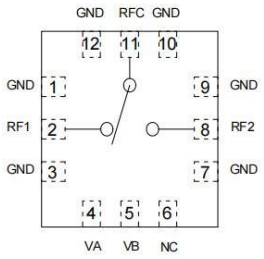
PRODUCT OVERVIEW:

The **LF-SP2T-20-GA** is a wideband, high isolation, low insertion loss, absorptive, double-throw (SP2T) switch. The **LF-SP2T-20-GA** operates from DC to 20 GHz with an insertion loss of lower than 1.8 dB and isolation of around 40 dB. The **LF-SP2T-20-GA** adopts 0/-5v logic control without external power supply bias and no power consumption. It has excellent switch characteristics and port VSWR characteristics in the working frequency band, and Compliant 3x3x1.2 mm QFN package.

KEY FEATURES:

- Ultra Wide Band: DC-20GHz
- Insertion Loss:1.8dB@20GH
- Isolation: >40dB@20GHz
- Compliant 3x31.2 mm QFN package

FUNCTION BLOCK DIOGRAM:



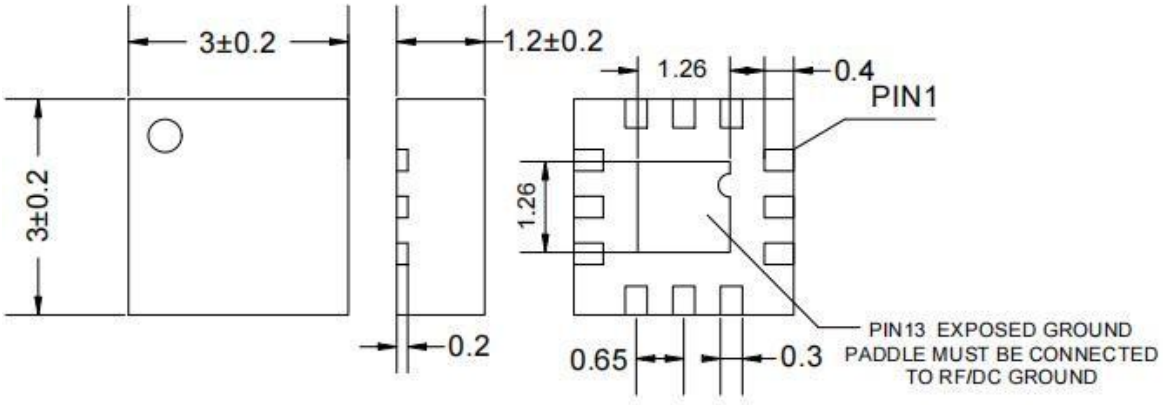
ELECTRICAL SPECIFICATIONS: (TA=+25℃, Control Voltage = 0/-5V):

Parameter		Min	Typ	Max	Units
Frequency range			DC-20		GHz
Insertion Loss	0.01-20GHz		1.8		dB
Isolation	0.01-20GHz	**40**	50		dBm
Return Loss RFC, RF1, RF2 (ON)	0.01-20GHz		-15		dB
Return Loss RF1, RF2 (OFF)	0.01-20GHz		-20		dB
Switch Time (50% VCTL to 90% of RF output)				20	ns

ABSOLUTE MAXIMUM RAITINGS:

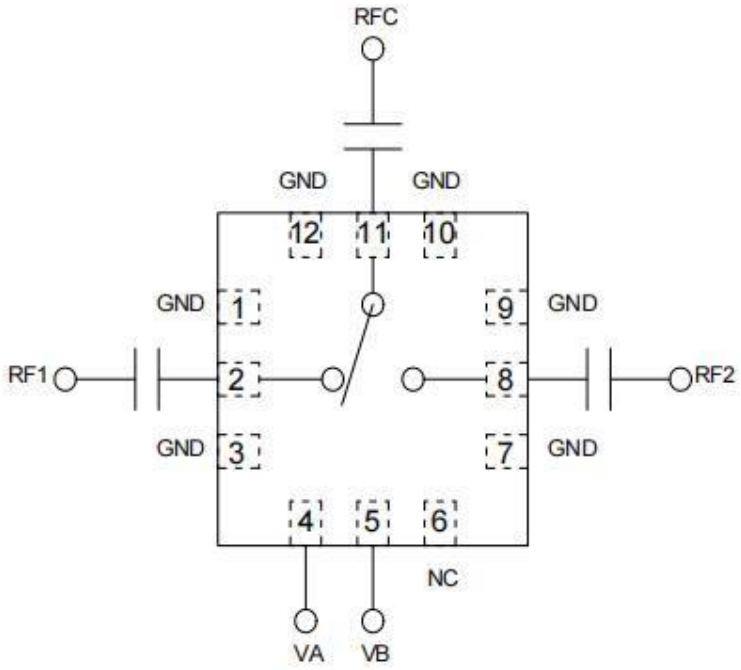
Parameter	Value
Input Power(1-20GHz)	27 dBm
Control Voltage	0~0.2V(Low) -3~-6V(High)
Channel temperature	150℃
Operating Temperature	-40℃ ~ +85℃
Non-operating Temperature	-65℃ ~ +150℃

OUTLINE & PORT SIZE: **Unit: mm**



TRUTH TABLE			
Control Input		Signal Path State	
VA	**VB**	**RFC-RF1**	**RFC-RF2**
Low	High	ON	OFF
High	Low	OFF	ON

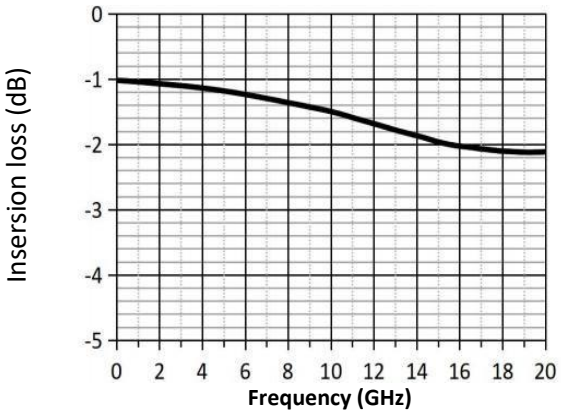
SUGGESTED ASSEMBLY DRAWING:



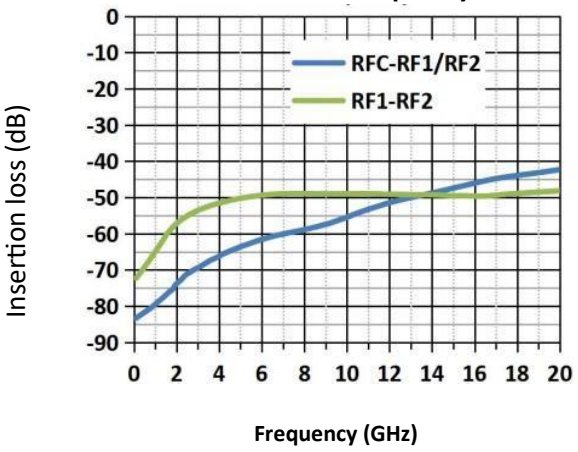
TYPICAL PERFORMANCE DATA:

Test Curves: TA = +25℃, Control Voltage = 0/-5V:

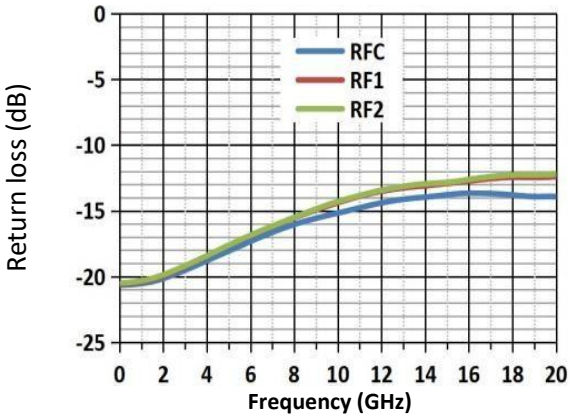
Insertion Loss vs Frequency



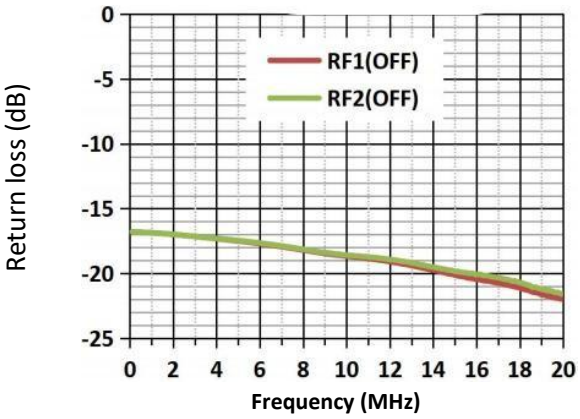
Isolation vs Frequency



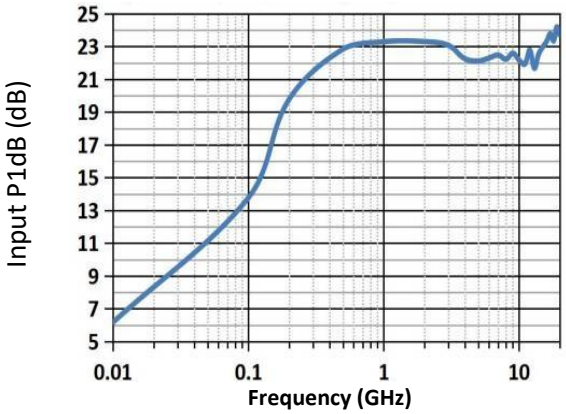
Return loss vs Frequency



Return loss vs Frequency



Input P1dB vs Frequency



Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environment and other factors like material lots etc.

APPLICATION INFORMATION:

1. Storage: The chip must be placed in a container with electrostatic protection function and stored in nitrogen environment.
2. Cleaning: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid detergent to clean the chip.
3. Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
4. Routine operation: Please use vacuum chuck or precision pointed tweezers to take the chip. Avoid touching the chip surface with tools or fingers during operation.
5. Power on sequence: when power on, apply gate voltage first and then Drain voltage; When de energizing, remove the Drain voltage first and then the gate voltage.
6. Mounting operation: The chip can be installed by AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat, and the gap between the chip and the input / output RF connecting line substrate shall be as small as possible.
7. Sintering process: 80 / 20 AuSn shall be used for sintering. The sintering temperature shall not exceed 300 ℃, the sintering time shall be as short as possible, not more than 20 seconds, and the friction time shall not exceed 3 seconds.
8. Bonding process: The dispensing amount of conductive adhesive shall be minimized during bonding, and the curing conditions shall refer to the data provided by the conductive adhesive manufacturer.
9. Bonding operation: Unless otherwise specified, two bonding wires (diameter 25um gold wire) are used for RF input and output, and the bonding wire shall be as short as possible.
The thermal ultrasonic bonding temperature is 150 ℃, and the ultrasonic energy is as small as possible. The pressure of spherical bonding cleaver is 40 ~ 50gf, and the pressure of wedge bonding cleaver is 18 ~ 22gf.
10. If you have any questions, please contact us at sales@lauftex.ru or visit our website http://lauftex.ru.